thickness of at least 5 micrometers.

28. A semiconductor wafer as in claim 11, wherein said chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center.--

REMARKS

Claims 5 and 10-28 are pending in the application. Claims 1-4 and 6-9 are canceled, above, in response to the Examiner's final restriction requirement. Additionally, new claims 12-28 are added, above, to further define Applicants' invention.

Claims 5, 10, and 11 stand rejected under 35 U.S.C.§ 102 (b) as being anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Steitz (United States Patent 3,719,981). Applicants respectfully traverse this rejection based on the following discussion.

I. Applicants' Claimed Invention

Applicants' invention, as defined by independent claims 5, 10 and 11 and shown in Figure 4A-4C is a semiconductor wafer 10 having a number of semiconductor chips or chip sections 10a defined thereon by scribe lines 13. Each chip section 10a has bump electrodes 70 formed thereon. Each chip section 10a has a number of chip electrodes 11 formed thereon.

A key feature of the claimed invention is the interconnection layers 60 which electrically connect the chip electrodes 11 and the bump electrodes 70 and the bump electrodes 70 being located other than the place just over the chip electrodes 11. More specifically, as defined by independent claim 5, the feature of "a plurality of interconnection layers, each of said interconnection layers including a first end connected to a bump electrode of said bump electrodes and

a second end connected a corresponding chip electrode of said chip electrodes, each of said bump electrodes being located at a position other than over said corresponding chip electrode" reduces the melting of the chip electrodes during the formation of the bump electrodes, as described on page 18, lines 20-23 of the application.

II. The Steitz Reference

Steitz is directed to a method of joining solder balls to solder bumps and discloses, as illustrated in Figure 5, a semiconductor wafer 2 divided into individual devices by dotted lines 14 and 16 where saw cuts will later be made. The semiconductor wafer 2 has solder bump connections 12. As shown in Figure 9, each solder ball 26 directly contacts one of the solder bumps 12. In other words, the solder balls 26 are located just over the solder bumps 12.

However, Steitz does not teach or suggest the interconnection layers 60 or the different locations of the bump electrodes and the chip electrodes, as defined by independent claims 5, 10 and 11 of the present application. More specifically, Steitz does not teach or suggest the feature of "a plurality of interconnection layers, each of said interconnection layers including a first end connected to a bump electrode of said bump electrodes and a second end connected a corresponding chip electrode of said chip electrodes, each of said bump electrodes being located at a position other than over said corresponding chip electrode", as defined by independent claim 5 and similarly defined by independent claims 10 and 11.

With the claimed invention the bump electrodes are not located directly over the chip electrodes which reduces the melting of the chip electrodes during the formation of the bump electrodes and provides a semiconductor wafer which is higher in quality and more efficient to manufacture than conventional semiconductor wafers, as described on page 18, lines 20-page 19, line 12 of the application.

Therefore, Applicants invention, as defined by independent claims 5, 10 and 11 is not anticipated or rendered obvious by Steitz and the Examiner is respectfully requested to reconsider and withdraw this rejection.

Further, new claims 12-28 are similarly not taught or suggested by the prior art of record and are similarly patentable.

III. Formal Matters and Conclusion

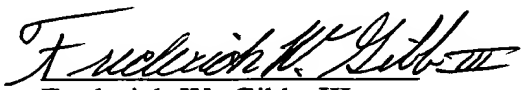
Turning to formal matters, a minor error in the specification has been corrected.

In view of the foregoing, Applicants submit that claims 5 and 10-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

If any extension of time is required with this document, Applicants hereby make a written conditional petition for extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 23-1951.

Respectfully submitted,



Frederick W. Gibb, III
Reg. No. 37,629

Whitham, Curtis, Whitham & McGinn
Reston International Center
11800 Sunrise Valley Dr., Suite 900
Reston, Virginia 20191
(703) 391-2510